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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,273	HAMERSLEY, RICHARD ALAN	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-11,23-25 and 31* is/are allowed.

6)☒ Claim(s) *1-5,7,12-21,26-30 and 32-42* is/are rejected.

7)☒ Claim(s) *6 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 7, 12-21, 26-30, 32, 33, and 36-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Cooper, US Patent Application Publication no. 2003/0120961.

Regarding claim 1, Cooper discloses a method of operating a computer system comprising:

determining if any performance state data stored in the computer system in a first area of memory specifying performance states for a plurality of processors and is associated with a processor being utilized in the computer system [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

if a portion of the performance state data is found to be associated with the processor being utilized in the computer system, copying the portion of the performance state data into a second area of memory [copy processor performance table to local table, Figure 4 and paragraph 0045].

Regarding claim 2, Cooper further discloses that the performance state data is stored in performance state tables [paragraphs 0044 and 0045].

Regarding claim 3, Cooper further discloses that the method is performed in a portion of basic input output system (BIOS) and wherein the first area of memory is a memory segment utilized during power on self test (POST) processing by BIOS and wherein the second area of memory is a runtime memory segment of BIOS [paragraphs 0040, 0044 and 0045].

Regarding claim 5, Cooper further discloses that when the portion of the performance state data is found to be associated with the processor being utilized in the computer system, computer identification information associated with the portion of the performance state data matches computer identification information in the processor [paragraphs 0044 and 0045].

Regarding claim 7, Cooper further discloses copying default performance state table data into local memory when no match is found [Figure 4 and paragraph 0045].

Regarding claim 12, Cooper discloses a method of operating a computer system comprising:

determining if any performance state data stored in the computer system specifying performance states for a plurality of processors is associated with a processor being utilized in the computer system [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

generating performance state data if none of the performance state data is associated with the processor being utilized in the computer system [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Regarding claim 13, Cooper further discloses copying default performance state table data into local memory when no match is found [Figure 4 and paragraph 0045].

Regarding claim 14, Cooper further discloses that the generating the performance state data further comprises generating performance state information including a plurality of frequency values and a fixed voltage value [paragraph 0038].

Regarding claim 15, Cooper further discloses that an upper limit of frequency of the frequency values is determined according to providing an indication of maximum frequency in the processor [paragraph 0038].

Regarding claim 16, Cooper further discloses that the plurality of frequency values are spread approximately evenly between a lower limit and the upper limit [paragraph 0038].

Regarding claim 17, Cooper discloses a computer program product stored on computer readable medium operable in a computer system to:

determine whether a match exists between a processor being utilized in the computer system and performance state information stored in a first area of memory [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

if a match exists, copying matching performance state information into a second area of memory, wherein the first area of memory is a memory segment utilized during power on self test (POST) processing by basic input output system (BIOS) and wherein the second area of memory is a runtime memory segment of BIOS [copy processor performance table to local table, Figure 4 and paragraphs 0040, 0044 and 0045].

Regarding claim 18, Cooper further discloses generating a performance state data after no match is found to exist between any of the performance state data and the processor being utilized in the computer system [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Regarding claim 19, Cooper further discloses copying default performance state table data into local memory when no match is found [Figure 4 and paragraph 0045].

Regarding claim 20, Cooper further discloses that the generating the performance state data further comprises generating performance state information including a plurality of frequency values and a fixed voltage value [paragraph 0038].

Regarding claim 21, Cooper further discloses that the plurality of frequency values are spread approximately evenly between a lower limit and the upper limit [paragraph 0038].

Regarding claim 26, Cooper discloses a computer program product stored on computer readable medium operable in a computer system to:

determine whether a match exists between a processor being utilized in the computer system and performance state information for a plurality of processors [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

generate performance state data after no match is found to exist [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Regarding claim 27, Cooper further discloses that the generating the performance state data further comprises generating performance state information including a plurality of frequency values and a fixed voltage value [paragraph 0038].

Regarding claim 28, Cooper further discloses that an upper limit of frequency of the frequency values is determined according to providing an indication of maximum frequency in the processor [paragraph 0038].

Regarding claim 29, Cooper further discloses that the plurality of frequency values are spread approximately evenly between a lower limit and the upper limit [paragraph 0038].

Regarding claim 30, Cooper discloses an apparatus comprising:

means for determining if any performance state data specifying performance states for a plurality of processors, which is stored in a first area of memory of a computer system utilized for system boot, is associated with a processor being utilized in the computer system [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

means for copying a portion of the performance state data into a second area of memory if the portion of the performance state data is found to be associated with the processor being utilized in the computer system [copy processor performance table to local table, Figure 4 and paragraphs 0040, 0044 and 0045].

Regarding claim 32, Cooper discloses an apparatus comprising:

means for determining if any performance state data stored in the computer system specifying performance states for a plurality of processors is associated with a processor being utilized in the computer system [scan through performance tables stored in BIOS, Figure 4 and paragraph 0045]; and

means for generating performance state data if none of the performance state data is associated with the processor being utilized in the computer system [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Regarding claim 33, Cooper discloses a computer program product stored on one or more computer readable media, operable in a computer system to:

copy one of a plurality of performance state data associated with respective processors from a disposable memory segment into a runtime memory segment [copy processor performance table to local table, Figure 4 and paragraphs 0040, 0044 and 0045]; and

generate an advanced configuration and power interface object based at least in part on the copied performance state data [paragraph 0041].

Regarding claim 36, Cooper further discloses that the method is performed in a portion of basic input output system (BIOS) and wherein the first area of memory is a memory segment utilized during power on self test (POST) processing by BIOS and wherein the second area of memory is a runtime memory segment of BIOS [paragraphs 0040, 0044 and 0045].

Regarding claim 37, Cooper further discloses that the copied performance state data has been determined to match a set of processor parameters that correspond to a processor in the computer system [Figure 4 and paragraph 0045].

Regarding claim 38, Cooper further discloses generating a performance state data after no match is found to exist between any of the plurality of performance state data and the processor being utilized in the computer system [copying default performance state table data into local memory when no match is found, Figure 4 and paragraph 0045].

Regarding claim 39, Cooper further discloses that the generating the performance state data further comprises generating performance state information including a plurality of frequency values and a fixed voltage value [paragraph 0038].

Regarding claim 40, Cooper discloses a computer system comprising:

memory that hosts a basic input/output system (BIOS) that selects a first of a plurality of performance state information from a first area of memory into a second area of memory,

wherein the first area of memory is to be utilized during power on self test (POST) processing by the BIOS, and wherein the second area of memory is to be used for a runtime memory segment of BIOS [Figure 4 and paragraphs 0040, 0044 and 0045]; and

a processor coupled with the memory [Figure 1].

Regarding claim 41, Cooper further discloses that the first performance state information corresponds to a set of one or more processor parameters that correspond to the processor [paragraphs 0044 and 0045].

Regarding claim 42, Cooper further discloses that the BIOS selects the first performance state information as exactly matching the set of processor parameter [paragraph 0045].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper, US Patent Application Publication no. 2003/0120961.

Regarding claim 4, Cooper, as described above, discloses a method comprising determining if a portion of the performance state data is found to be associated with a processor being utilized in the computer system and, if so, copying a portion of the performance state data into a second area of memory. Cooper is silent regarding to the start address the second area of memory. Examiner takes official notice that the address 0xF000 is a conventional choice as a

start address for a runtime memory segment. It would have been obvious to one of ordinary skill in the art to use the conventional address 0xF000 as the starting address for storing the copy of the portion of the performance state data in the Cooper method.

Regarding claims 34 and 35, Cooper discloses generating the CPI objects dynamically [paragraph 0041]. Applicant's numerous definitions of a how the ACPI object is generated (claims 34 and 35) is construed to be an admission that the criticality does not reside in how the ACPI object is generated and hence are obvious variations of one another.

Allowable Subject Matter

Claims 8-11, 23-25 and 31 are allowed.

Claims 6, 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dwyer, III et al., US Patent Application Publication no. 2004/0054936, discloses looking up an optimal core voltage for a processor based on the processor type.

Dreyer et al., US Patent no. 5,958,037, discloses identifying features of processor based on the processor type.

Washington et al., US Patent no. 5,835,775, discloses a method for determining functionality of a processor based on the processor type.

Alpert et al., US Patent no. 5,671,435, discloses a method for determining features implemented in a processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LYNNE H. BROWNE
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Paul Yanchus
August 16, 2006